CLAIMS:

The invention claimed is:

1. A method of depositing a silicon dioxide comprising layer in the fabrication of integrated circuitry, comprising:

providing a semiconductor substrate having an exposed outer first surface comprising silicon-nitrogen bonds and an exposed outer second surface comprising at least one of silicon and silicon dioxide;

depositing a layer comprising a metal over at least the outer second surface; and

flowing a silanol to the metal of the outer second surface and to the outer first surface effective to selectively deposit a silicon dioxide comprising layer over the outer second surface as compared to the outer first surface.

2. The method of claim 1 wherein the metal comprises a metal compound.

3. The method of claim 1 wherein the metal comprises one of aluminum, yttrium, zirconium, hafnium and mixtures thereof.

4. The method of claim 3 wherein the metal comprises aluminum.

5. The method of claim 3 wherein the metal comprises a metal compound.

6. The method of claim 5 wherein the metal compound comprises aluminum.

7. The method of claim 5 wherein the metal compound comprises a methyl aluminum.

8. The method of claim 5 wherein the metal compound comprises aluminum oxide.

9. The method of claim 1 wherein the outer second surface comprises silicon.

10. The method of claim 9 wherein the silicon comprises monocrystalline silicon.

11. The method of claim 9 wherein the silicon comprises polycrystalline silicon.

12. The method of claim 1 wherein the metal comprising layer is no more than 4 monolayers thick.

13. The method of claim 1 wherein the outer second surface comprises silicon dioxide.

14. The method of claim 1 wherein said flowing of silanol is continuous.

15. The method of claim 1 wherein said flowing of silanol is continuous at a substantially constant rate.

16. The method of claim 1 wherein said flowing of silanol is pulsed.

17. The method of claim 1 wherein the silanol comprises an alkoxysilanol.

18. The method of claim 17 wherein the silanol comprises tristertbutoxysilanol.

19. The method of claim 17 wherein the silanol comprises tristertbutoxysilanol, and the metal comprises an aluminum compound deposited from a methyl aluminum precursor.

20. The method of claim 17 wherein the silanol comprises tristertbutoxysilanol, and the metal comprises an aluminum compound deposited from trimethyl aluminum.

21. The method of claim 1 wherein the selective deposit is self limiting to silicon dioxide comprising deposition after completing said depositing the layer comprising the metal.

22. The method of claim 1 wherein the selective deposit is self limiting to silicon dioxide comprising deposition after completing said depositing the layer comprising the metal, and further comprising repeating said depositing the layer comprising the metal and said flowing the silanol at least once.

23. The method of claim 1 wherein the silanol is flowed to the substrate at a substrate temperature of from 200°C to 300°C.

24. The method of claim 1 wherein the silicon dioxide comprising layer is substantially amorphous.

25. The method of claim 1 wherein the selective deposit is at a ratio of at least 5:1.

26. The method of claim 1 wherein the selective deposit is at a ratio of at least 10:1.

27. The method of claim 1 wherein the selective deposit is at a ratio of at least 50:1.

28. The method of claim 1 wherein the selective deposit is at a ratio of at least 99:1 for at least the first 100 Angstroms of thickness of the silicon dioxide comprising layer.

29. The method of claim 1 wherein the selective deposit is at a ratio of at least 99:1 for at least the first 250 Angstroms of thickness of the silicon dioxide comprising layer.

30. The method of claim 1 wherein the exposed outer first surface comprises silicon nitride.

31. The method of claim 1 wherein the exposed outer first surface comprises silicon oxynitride.

32. The method of claim 1 comprising fabricating logic circuitry.

33. The method of claim 1 comprising fabricating an array of memory cells.

34. The method of claim 1 wherein the depositing the layer comprising metal is selective over the outer second surface as compared to the outer first surface.

35. The method of claim 34 comprising treating at least the outer second surface prior to said depositing effective to enhance the selective depositing of the layer comprising metal to deposit over the outer second surface as compared to the outer first surface.

36. The method of claim 35 wherein the treating comprises exposure to H_2O.

37. The method of claim 36 wherein the metal comprises an aluminum metal compound.

38. The method of claim 37 wherein the aluminum metal compound comprises methyl aluminum.

39. The method of claim 37 wherein the aluminum metal compound comprises aluminum oxide.

40. The method of claim 37 wherein the aluminum metal compound comprises methyl aluminum and aluminum oxide.

41. A method of forming trench isolation in the fabrication of integrated circuitry, comprising:

forming a masking layer comprising silicon-nitrogen bonds over a semiconductor substrate;

etching isolation trenches through the masking layer into semiconductive material of the semiconductor substrate;

providing the masking layer to have an exposed elevationally outermost first surface comprising silicon-nitrogen bonds, and providing the isolation trenches within the semiconductor substrate to comprise an exposed second surface comprising at least one of silicon and silicon dioxide;

depositing a layer comprising a metal over at least the outer second surface; and

flowing a silanol to the metal of the outer second surface and to the outer first surface effective to selectively deposit a silicon dioxide comprising layer over the outer second surface as compared to the outer first surface.

42. The method of claim 41 wherein the providing comprises:

forming a silicon nitride comprising trench liner over semiconductive material sidewalls and semiconductive material bases of the isolation trenches; and

anisotropically etching through the trench liner over the trench bases and effective to leave the trench liner over the trench sidewalls.

43. The method of claim 41 wherein the selectively depositing is effective to fill the isolation trenches within semiconductive material of the semiconductive substrate.

44. The method of claim 43 wherein the selectively depositing relative to the isolation trenches is effective to no more than fill the isolation trenches within semiconductive material of the semiconductive substrate.

45. The method of claim 41 wherein the metal comprises a metal compound.

46. The method of claim 41 wherein the metal comprises one of aluminum, yttrium, zirconium, hafnium and mixtures thereof.

47. The method of claim 46 wherein the metal comprises aluminum.

48. The method of claim 46 wherein the metal comprises a metal compound.

49. The method of claim 48 wherein the metal compound comprises aluminum.

50. The method of claim 48 wherein the metal compound comprises a methyl aluminum.

51. The method of claim 48 wherein the metal compound comprises aluminum oxide.

52. The method of claim 41 wherein the outer second surface comprises silicon.

53. The method of claim 41 wherein the outer second surface comprises silicon dioxide.

54. The method of claim 41 wherein the silanol comprises an alkoxysilanol.

55. The method of claim 54 wherein the silanol comprises tristertbutoxysilanol.

56. The method of claim 54 wherein the silanol comprises tristertbutoxysilanol, and the metal comprises an aluminum compound deposited from a methyl aluminum precursor.

57. The method of claim 54 wherein the silanol comprises tristertbutoxysilanol, and the metal comprises an aluminum compound deposited from trimethylaluminum.

58. The method of claim 41 wherein the selective deposit is self limiting to silicon dioxide comprising deposition after completing said depositing the layer comprising the metal.

59. The method of claim 41 wherein the selective deposit is self limiting to silicon dioxide comprising deposition after completing said depositing the layer comprising the metal, and further comprising repeating said depositing the layer comprising the metal and said flowing the silanol at least once.

60. The method of claim 41 wherein the metal comprising layer is no more than 4 monolayers thick.

61. The method of claim 41 wherein the exposed elevationally outermost first surface comprises silicon nitride.

62. The method of claim 41 wherein the exposed elevationally outermost first surface comprises silicon oxynitride.

63. A method of forming trench isolation in the fabrication of integrated circuitry, comprising:

forming a masking layer comprising silicon-nitrogen bonds over a semiconductor substrate;

etching isolation trenches through the masking layer into semiconductive material of the semiconductor substrate;

forming a silicon nitride comprising trench liner over semiconductive material sidewalls and semiconductive material bases of the isolation trenches;

anisotropically etching through the trench liner over the trench bases and effective to leave the trench liner over the trench sidewalls;

providing the masking layer to have an exposed elevationally outermost first surface comprising silicon-nitrogen bonds, and providing the isolation trench bases to comprise an exposed second surface comprising at least one of silicon and silicon dioxide; and

selectively depositing a silicon dioxide comprising layer over the second surface as compared to the outer first surface.

64. The method of claim 63 wherein the silicon nitride comprising trench liner is formed on the semiconductive material sidewalls and on the semiconductive material bases.

65. The method of claim 63 wherein the selectively depositing comprises flowing a silanol to the substrate.

66. The method of claim 63 wherein the selectively depositing is effective to fill the isolation trenches within semiconductive material of the semiconductive substrate.

67. The method of claim 66 wherein the selectively depositing relative to the isolation trenches is effective to no more than fill the isolation trenches within semiconductive material of the semiconductive substrate.

68. The method of claim 63 wherein the outer second surface comprises silicon.

69. The method of claim 63 wherein the outer second surface comprises silicon dioxide.

70. The method of claim 63 wherein the silanol comprises an alkoxysilanol.

71. The method of claim 70 wherein the silanol comprises tristertbutoxysilanol.

72. The method of claim 63 wherein the selective deposit is self limiting to silicon dioxide comprising deposition after completing said depositing the layer comprising the metal.

73. The method of claim 63 wherein the selective deposit is self limiting to silicon dioxide comprising deposition after completing said depositing the layer comprising the metal, and further comprising repeating said depositing the layer comprising the metal and said flowing the silanol at least once.

74. The method of claim 63 wherein the metal comprising layer is no more than 4 monolayers thick.

75. The method of claim 63 wherein the exposed elevationally outermost first surface comprises silicon nitride.

76. The method of claim 63 wherein the exposed elevationally outermost first surface comprises silicon oxynitride.

77. A method of depositing a silicon dioxide comprising layer in the fabrication of integrated circuitry, comprising:

providing a semiconductor substrate having a field effect transistor gate construction, the gate construction comprising an insulative cover comprising an exposed outer first surface comprising silicon-nitrogen bonds;

providing the semiconductor substrate to comprise an exposed outer second surface proximate the gate construction comprising at least one of silicon and silicon dioxide; and

flowing a gaseous silicon containing precursor and a gaseous oxygen containing precursor to the first and second surfaces effective to selectively deposit a substantially undoped silicon dioxide comprising diffusion barrier layer over the outer second surface as compared to the outer first surface.

78. The method of claim 77 further comprising depositing a doped silicon dioxide comprising layer on the substantially undoped silicon dioxide comprising layer.

79. The method of claim 77 wherein the silicon comprising precursor comprises a silanol.

80. The method of claim 77 wherein the oxygen and silicon containing precursors are a single precursor.

81. The method of claim 77 wherein the oxygen and silicon containing precursors are at least two precursors.

82. The method of claim 77 comprising depositing a layer comprising a metal over at least the outer second surface, and wherein the silicon comprising precursor comprises a silanol.

83. The method of claim 82 wherein the metal comprises a metal compound.

84. The method of claim 82 wherein the metal comprises one of aluminum, yttrium, zirconium, hafnium and mixtures thereof.

85. The method of claim 84 wherein the metal comprises aluminum.

86. The method of claim 84 wherein the metal comprises a metal compound.

87. The method of claim 86 wherein the metal compound comprises aluminum.

88. The method of claim 86 wherein the metal compound comprises a methyl aluminum.

89. The method of claim 86 wherein the metal compound comprises aluminum oxide.

90. The method of claim 82 wherein the outer second surface comprises silicon.

91. The method of claim 82 wherein the outer second surface comprises silicon dioxide.

92. The method of claim 82 wherein the silanol comprises an alkoxysilanol.

93. The method of claim 92 wherein the silanol comprises tristertbutoxysilanol.

94. The method of claim 92 wherein the silanol comprises tristertbutoxysilanol, and the metal comprises an aluminum compound deposited from a methyl aluminum precursor.

95. The method of claim 92 wherein the silanol comprises tristertbutoxysilanol, and the metal comprises an aluminum compound deposited from trimethylaluminum.

96. The method of claim 82 wherein the selective deposit is self limiting to silicon dioxide comprising deposition after completing said depositing the layer comprising the metal.

97. The method of claim 82 wherein the selective deposit is self limiting to silicon dioxide comprising deposition after completing said depositing the layer comprising the metal, and further comprising repeating said depositing the layer comprising the metal and said flowing the silanol at least once.

98. The method of claim 77 wherein the exposed outer first surface comprises silicon nitride.

99. The method of claim 77 wherein the exposed outer first surface comprises silicon oxynitride.

100. The method of claim 77 wherein the gate construction comprises a conductive region, the insulative cover covering all outer surfaces of the conductive region.

101. A method of depositing a silicon dioxide comprising layer in the fabrication of integrated circuitry, comprising:

providing a semiconductor substrate having a pair of spaced conductive line constructions, the conductive line constructions respectively comprising an insulative cap and conductive region sidewalls, the insulative cap comprising an exposed outer first surface comprising silicon-nitrogen bonds, one of the conductive region sidewalls of one of the conductive line constructions facing one of the conductive region sidewalls of the other conductive line construction, the facing conductive region sidewalls being outwardly exposed;

providing the semiconductor substrate to comprise an exposed outer second surface extending between the pair of conductive line constructions, the exposed outer second surface comprising at least one of silicon and silicon dioxide; and

flowing a gaseous silicon containing precursor and a gaseous oxygen containing precursor to the first and second surfaces effective to selectively deposit a silicon dioxide comprising layer over the outer second surface as compared to the outer first surface to cover the facing conductive region sidewalls.

102. The method of claim 101 wherein the silicon comprising precursor comprises a silanol.

103. The method of claim 101 wherein the oxygen and silicon containing precursors are a single precursor.

104. The method of claim 101 wherein the oxygen and silicon containing precursors are at least two precursors.

105. The method of claim 101 comprising depositing a layer comprising a metal over at least the outer second surface, and wherein the silicon comprising precursor comprises a silanol.

106. The method of claim 105 wherein the metal comprises a metal compound.

107. The method of claim 105 wherein the metal comprises one of aluminum, yttrium, zirconium, hafnium and mixtures thereof.

108. The method of claim 107 wherein the metal comprises aluminum.

109. The method of claim 107 wherein the metal comprises a metal compound.

110. The method of claim 109 wherein the metal compound comprises aluminum.

111. The method of claim 109 wherein the metal compound comprises a methyl aluminum.

112. The method of claim 109 wherein the metal compound comprises aluminum oxide.

113. The method of claim 105 wherein the outer second surface comprises silicon.

114. The method of claim 105 wherein the outer second surface comprises silicon dioxide.

115. The method of claim 105 wherein the silanol comprises an alkoxysilanol.

116. The method of claim 115 wherein the silanol comprises tristertbutoxysilanol.

117. The method of claim 115 wherein the silanol comprises tristertbutoxysilanol, and the metal comprises an aluminum compound deposited from a methyl aluminum precursor.

118. The method of claim 115 wherein the silanol comprises tristertbutoxysilanol, and the metal comprises an aluminum compound deposited from trimethylaluminum.

119. The method of claim 105 wherein the selective deposit is self limiting to silicon dioxide comprising deposition after completing said depositing the layer comprising the metal.

120. The method of claim 105 wherein the selective deposit is self limiting to silicon dioxide comprising deposition after completing said depositing the layer comprising the metal, and further comprising repeating said depositing the layer comprising the metal and said flowing the silanol at least once.

121. The method of claim 101 wherein the exposed outer first surface comprises silicon nitride.

122. The method of claim 101 wherein the exposed outer first surface comprises silicon oxynitride.

123. The method of claim 101 wherein the conductive line constructions comprise field effect transistor gate constructions.

124. A method of forming a bit line over capacitor array of memory cells, comprising:

forming a layer comprising silicon-nitrogen bonds over an outer capacitor cell electrode;

etching bit contact openings through the layer comprising silicon-nitrogen bonds and through the outer capacitor cell electrode;

providing the layer comprising silicon-nitrogen bonds to have an exposed elevationally outer first surface comprising silicon-nitrogen bonds, and providing the bit contact openings to comprise bases comprising an exposed second surface comprising at least one of silicon and silicon dioxide; and

selectively depositing a silicon dioxide comprising layer over the outer second surface as compared to the outer first surface.

125. The method of claim 124 wherein the outer capacitor cell electrode comprises polysilicon.

126. The method of claim 124 wherein the outer capacitor cell electrode comprises polysilicon, and a sidewall of which is exposed during the selectively depositing; and

the selectively depositing forming the silicon dioxide comprising layer over the outer surface as compared to the exposed sidewall.

127. The method of claim 124 wherein the selectively depositing comprises:

depositing a layer comprising a metal over at least the outer second surface; and

flowing a silanol to the metal of the outer second surface and to the outer first surface.

128. The method of claim 127 wherein the metal comprises a metal compound.

129. The method of claim 127 wherein the metal comprises one of aluminum, yttrium, zirconium, hafnium and mixtures thereof.

130. The method of claim 129 wherein the metal comprises aluminum.

131. The method of claim 129 herein the metal comprises a metal compound.

132. The method of claim 131 wherein the metal compound comprises aluminum.

133. The method of claim 131 wherein the metal compound comprises a methyl aluminum.

134. The method of claim 131 wherein the metal compound comprises aluminum oxide.

135. The method of claim 127 wherein the outer capacitor cell electrode is formed over a capacitor dielectric region, the etching forming the bit contact openings entirely through the capacitor dielectric region prior to the selectively depositing such that the exposed second surface comprises an insulative layer beneath the capacitor dielectric region.

136. The method of claim 127 wherein the outer capacitor cell electrode is formed over a capacitor dielectric region, the etching stopping on the capacitor dielectric region such that the bit contact openings do not extend entirely through the capacitor dielectric region prior to the selectively depositing and such that the exposed second surface comprises the capacitor dielectric region.

137. The method of claim 127 wherein the outer second surface comprises silicon.

138. The method of claim 127 wherein the outer second surface comprises silicon dioxide.

139. The method of claim 127 herein the silanol comprises an alkoxysilanol.

140. The method of claim 139 wherein the silanol comprises tristertbutoxysilanol.

141. The method of claim 139 wherein the silanol comprises tristertbutoxysilanol, and the metal comprises an aluminum compound deposited from a methyl aluminum precursor.

142. The method of claim 139 wherein the silanol comprises tristertbutoxysilanol, and the metal comprises an aluminum compound deposited from trimethylaluminum.

143. The method of claim 127 wherein the selective deposit is self limiting to silicon dioxide comprising deposition after completing said depositing the layer comprising the metal.

144. The method of claim 127 wherein the selective deposit is self limiting to silicon dioxide comprising deposition after completing said depositing the layer comprising the metal, and further comprising repeating said depositing the layer comprising the metal and said flowing the silanol at least once.

145. The method of claim 127 wherein the exposed outer first surface comprises silicon nitride.

146. The method of claim 127 wherein the exposed outer first surface comprises silicon oxynitride.

147. A method of forming a bit line over capacitor array of memory cells, comprising:

forming a layer comprising silicon-nitrogen bonds over an outer capacitor cell electrode, the outer capacitor electrode comprising polysilicon;

etching bit contact openings through the layer comprising silicon-nitrogen bonds and through the outer capacitor cell electrode;

providing the layer comprising silicon-nitrogen bonds to have an exposed elevationally outer first surface comprising silicon-nitrogen bonds, and providing the bit contact openings to comprise outer capacitor electrode sidewall portions comprising polysilicon; and

selectively depositing a silicon dioxide comprising layer over the polysilicon comprising sidewall portions as compared to the outer first surface.

148. The method of claim 147 wherein the selectively depositing comprises:

depositing a layer comprising a metal over at least the polysilicon comprising sidewall portions; and

flowing a silanol to the metal of the polysilicon comprising sidewall portions and to the outer first surface.

149. The method of claim 148 wherein the metal comprises a metal compound.

150. The method of claim 148 wherein the metal comprises one of aluminum, yttrium, zirconium, hafnium and mixtures thereof.

151. The method of claim 150 wherein the metal comprises aluminum.

152. The method of claim 150 herein the metal comprises a metal compound.

153. The method of claim 152 wherein the metal compound comprises aluminum.

154. The method of claim 152 wherein the metal compound comprises a methyl aluminum.

155. The method of claim 152 wherein the metal compound comprises aluminum oxide.

156. The method of claim 148 herein the silanol comprises an alkoxysilanol.

157. The method of claim 156 wherein the silanol comprises tristertbutoxysilanol.

158. The method of claim 156 wherein the silanol comprises tristertbutoxysilanol, and the metal comprises an aluminum compound deposited from a methyl aluminum precursor.

159. The method of claim 156 wherein the silanol comprises tristertbutoxysilanol, and the metal comprises an aluminum compound deposited from trimethylaluminum.

160. The method of claim 148 wherein the selective deposit is self limiting to silicon dioxide comprising deposition after completing said depositing the layer comprising the metal.

161. The method of claim 148 wherein the selective deposit is self limiting to silicon dioxide comprising deposition after completing said depositing the layer comprising the metal, and further comprising repeating said depositing the layer comprising the metal and said flowing the silanol at least once.

162. The method of claim 148 wherein the exposed outer first surface comprises silicon nitride.

163. The method of claim 148 wherein the exposed outer first surface comprises silicon oxynitride.

164. The method of claim 148 wherein the outer capacitor cell electrode is formed over a capacitor dielectric region, the etching forming the bit contact openings entirely through the capacitor dielectric region prior to the selectively depositing.

165. The method of claim 148 wherein the outer capacitor cell electrode is formed over a capacitor dielectric region, the etching stopping on the capacitor dielectric region such that the bit contact openings do not extend entirely through the capacitor dielectric region prior to the selectively depositing.